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POWER REDUCTION IN MODERN VLSI SYSTEMS: CHALLENGES AND INNOVATIONS IN CMOS TECHNOLOGY

OGGI SUDHAKAR[1], DR. SHARAD KUMAR [2]
DEPARTMENT OF SCHOOL OF ENGINEERING & TECHNOLOGY
[1,2]SHRI VENKATESHWARA UNIVERSITY, GAJRAULA (UTTAR PRADESH)

ABSTRACT

Advanced Low-Power Digital Circuit Techniques introduces many innovative high-performance digital circuit designs that prioritize low-power and low-voltage functionality. These circuits exemplify a diverse array of configurations used in cutting-edge VLSI systems, hence providing excellent illustrations for low-power design. The progression of Very Large-Scale Integration (VLSI) design has yielded substantial improvements in contemporary electronics. Power consumption in digital circuits, particularly those using Complementary Metal-Oxide-Semiconductor (CMOS) technology, has emerged as a significant challenge. This study examines the principles of low-power VLSI design, approaches for power reduction, and the problems presented by contemporary digitized CMOS technology. The research further assesses novel approaches for minimizing energy use while preserving performance efficacy.

Keywords: Low power digital circuit; High performance VLSI; Energy efficient CMOS; Emerging technologies; Power Optimization in VLSI

1. INTRODUCTION

Low power design encompasses a set of approaches and procedures intended to minimize both dynamic and static power consumption in an integrated circuit (IC). Companies are persistently advancing new features and functionalities, all integrated into portable, handheld, and battery-operated gadgets. The early stages of research and development in VLSI design focused on attaining both high speed and miniaturization. Currently, the increasing trends in portable computing and wireless applications need the exploration of novel technologies and the development of circuits that have low power consumption (Hussain and Chaudhury, 2020).

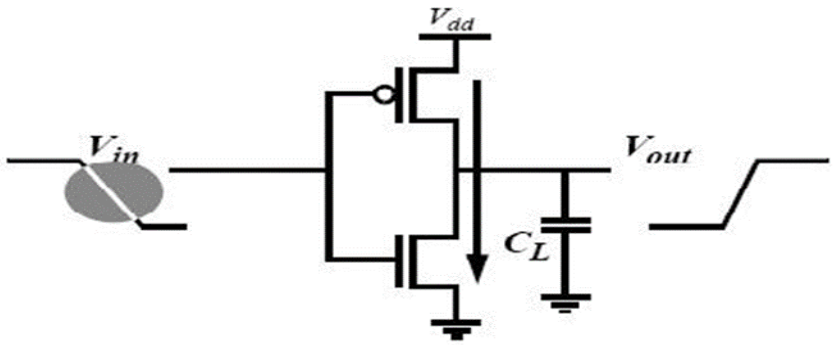

Figure 1: Low power VLSI chip design (Hussain and Chaudhury, 2020)

The disparity between the capacity of a hand-held device's battery and the amount of power it needs is becoming an increasingly important consideration for manufacturers of most portable hand-held wireless devices. In light of this, one of the most significant concerns in integrated circuit (IC) design is now the optimization of power consumption and energy efficiency. For modern integrated circuits (ICs), high speed, absolute precision, reliability, and low power consumption have been declared as the most important design goals (Hiramoto, 2019).

Thus, the advancement of CMOS technology has continuously resulted in the production of fast, compact, and power-efficient electronic devices. However, the increasing density of transistors on ICs has made power consumption a great concern (Munirathnam and Babu, 2021). Traditionally, VLSI designers were mainly concerned with speed, cost, and area at the expense of power efficiency. However, the very fact that portable devices are being used widely and energy-efficient computing have made the reduction of power consumption essential. The research aims to investigate various techniques and methodologies for reducing power consumption within VLSI circuits developed by using digitized CMOS technology. Topics involved include various significant issues such as dynamic power dissipation, leakage power, and power integrity concerns, and innovative design techniques in developing energy-efficient digital circuits (Kumar et al., 2020).

2. POWER REDUCTION TECHNIQUES IN CMOS VLSI DESIGN

Within these aspects of circuit power usage in VLSI, the consumption of power can be divided into two categories: dynamic and static power. The dynamic power dissipation associated with charging and discharging capacitors is also considered, whereas static power refers to leakage currents in transistors. Several approaches toward these solutions have already been sought to reduce the power consumed (Gubbi and Deeksha, 2016).

2.1 **Low Swing Clocking**

Clock activity accounts for a large portion of total power consumption in digital circuits. Low-swing clocking keeps the clock network voltage swing low, which reduces dynamic power dissipation. Utilizing low threshold voltage CMOS transistors minimizes performance loss while providing effective power savings.

2.2 Dual-Edge Triggering

Dual-edge triggering decreases the operating frequency of circuits while maintaining performance. Dual-edge triggering allows data sample on both the rising and falling edges of the clock signal, rather than collecting data just once each clock cycle. This decreases total power usage by around 50% while preserving throughput.

2.3 Clock Gating

Clock gating is a very efficient method for minimizing power consumption in digital circuitry. This technique deactivates the clock signal to non-operational circuit blocks, thereby minimizing superfluous switching activity and preserving energy.

2.4 Multiple Supply Voltage

A singular supply voltage considerably elevates power usage. Implementing several voltage domains inside a circuit allows transistors on key channels to receive elevated voltages for best performance, while non-critical paths function at reduced voltages to minimize power consumption.

2.5 Power Gating

Power gating mitigates leakage power by severing idle circuit blocks from the power source. This method utilizes high threshold voltage transistors to entirely disconnect the power supply to inactive portions of the device, thereby minimizing leakage currents.

2.6 Dynamic Voltage and Frequency Scaling (DVFS)

DVFS dynamically modifies the clock frequency and supply voltage in response to computing demands. Significant power savings result from lowering the supply voltage and frequency when high performance is not needed.

3. CHALLENGES IN LOW POWER VLSI DESIGN

Notwithstanding considerable progress in power reduction methodologies, several problems remain in the design and execution of low-power VLSI circuits (Geetha et al., 2017).

3.1 Increased Design Complexity

With the increasing need for power-efficient circuits, designers must include various power-saving strategies while maintaining overall system performance. This elevates circuit complexity and design burden (Bhuvana and Bhaaskaran, 2018).

3.2 Power Integrity Issues

Voltage reductions and noise-related issues occur as a result of heightened current flow in intricate circuits. Maintaining a steady power distribution network while ensuring electricity efficiency is a significant task.

3.3 Trade-offs Between Performance and Power

Improving power efficiency could oftentimes mean giving up performance. Achieving optimal energy consumption without compromising speed demands meticulous design and optimization of circuits (Archana et al., 2016).

3.4 Technology Scaling Limitations

With the continuous miniaturization of transistors, increased leakage flows lead to elevated static power dissipation, which proves its difficulty in controlling leakage power at the cost of high-performance levels in nanometer-scale technologies.

3.5 Heat Dissipation and Thermal Management

Increased energy density entails an increase in the amount of heat generated, creating a concern on circuit reliability and lifespan, all due to the general efficiency of the thermal management associated with spurious thermal management (Agha et al., 2017)

4. FUTURE TRENDS AND EMERGING SOLUTIONS

Research fronts out the lines of methodologies and new technologies to tackle the issues of low-power VLSI design.

4.1 Subthreshold and Near-Threshold Computing

Computing essentially operates transistors at subthreshold or near-threshold voltages when power needs are made to be very small. This method is mostly used for energy-efficient IoT end-node or edge computing applications (Adwani, et al., 2015).

4.2 Approximate Computing

In cases where precision is not essential, approximation computation methods sacrifice accuracy for enhanced power efficiency. This method is very efficient for image processing, machine learning, and sensor-driven applications.

4.3 Energy Harvesting Integration

Energy harvesting techniques such as solar cells or piezoelectric generators may be viable solutions for low-power requirements in VLSI circuits. The integration of energy-harvesting technologies into CMOS-based systems is a rapidly growing avenue of research (Amirsoleimani et al., 2020).

4.4 3D ICs and Heterogeneous Integration

Three-dimensional (3D) integrated circuits allow for vertical stacking of circuit elements to minimize interconnect delay and enhance power efficiency. Heterogeneous integration with various semiconductor technologies further improves performance while reducing power consumption.

5. CONCLUSION

VLSI design for minimum energy consumption forms an integral aspect of modern semiconductor technology. Thus, the demand for energy-efficient digital circuitry has propelled advanced power reduction techniques into the foreground. While various methods including clock gating, power gating, and DVFS may prove effective, limitations due to technological scaling and heat dissipation still prevail. After that come perspectives for the advance of sub-threshold computing, approximate computing, and energy harvesting as possible solutions to these difficulties. The semiconductor industry could eventually exploit this ongoing quest for lower power design practices for improving energy efficiency and sustainability of electronic products.

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